REMARKS

Claims 1-40 are all the claims presently pending in the application. Claims 2, 4, 15, 19, 26 and 31 have been amended to more clearly define the invention. Claims 1, 15 and 18 are independent

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claim 4 stands rejected upon informalities (e.g., 35 U.S.C. § 112, second paragraph). Claims 1-2, 4, 6-19, 22-31, 33 and 35-40 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Khouja et al. (U.S. Patent No. 5,682,320). Claims 3, 20 and 32 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Khouja et al., in view of "P1497 Draft Standard for Standard Delay Format", IEEE (hereinafter "the Standard Delay Format (SDF) publication"). Claims 5, 21 and 34 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Khouja et al., in view of Fallah-Tehrani et al. (U.S. Patent No. 6,405,348).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., defined by claim 1) is directed to a method of analyzing power distribution in an integrated circuit chip. The method includes dividing a clock cycle of the integrated circuit chip into a plurality of time periods, dividing the integrated circuit chip into a plurality of cells, performing a static timing analysis for the plurality of cells to obtain current waveform data for each cell and each time period, performing a power distribution analysis using the current waveform data.

Conventional methods of analyzing power distribution typically assume that all circuits are switching at the same time (Application at page 3, lines 1-5). However, this causes the chip to be over-designed. Other methods simulate functional patterns through the chip logic

(Application at page 3, lines 6-16). However, this requires numerous patterns and is, therefore, expensive.

The claimed invention, on the other hand, divides a clock cycle of the chip into a plurality of periods, divides the chip into a plurality of cells, and performs a static timing analysis for the plurality of cells to obtain current waveform data for each cell and each time period (Application at page 11, lines 1-18). This allows the claimed invention to perform a transient power distribution analysis, unlike the conventional methods which are only concerned with an average power condition.

II. THE 35 USC §112, SECOND PARAGRAPH REJECTION

Claim 4 stands rejected under 35 U.S.C. §112, second paragraph. The claims have been amended, above, to overcome this rejection. Specifically, claim 4 has been amended to depend from claim 2.

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

III. THE PRIOR ART REFERENCES

A. The Khouja Reference

The Examiner alleges that Khouja teaches the claimed invention of claims 1-2, 4, 6-19, 22-31, 33 and 35-40. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Khouja.

Khouja discloses a method of computing the power dissipated by a digital circuit using information available at the gate library level. It estimates the short-circuit power by modeling the energy dissipated by the cell per input transition as a function of the transition time or edge rate, and multiplying that value by the number of transitions per second for that input (Kouja at Abstract).

However, contrary to the Examiner's allegations, Khouja does not teach or suggest "*performing a static timing analysis for said plurality of cells to obtain current waveform data*

for each cell and each time period", as recited in claims 1 and 18, and similarly recited in claim 15.

As noted above, unlike conventional methods of analyzing power distribution, the claimed invention divides a clock cycle of the chip into a plurality of periods, divides the chip into a plurality of cells, and performs a static timing analysis for the plurality of cells to obtain current waveform data for each cell and each time period (Application at page 11, lines 1-18). This allows the claimed invention to perform a transient power distribution analysis, unlike the conventional methods which are only concerned with an average power condition.

Clearly, the novel features of the claimed invention are not taught or suggested by Khouja. Indeed, the Examiner attempts to rely on col. 10, line 45-col. 11 line 22 of Khouja to support his allegations. However, the Examiner is clearly incorrect.

This passage in Khouja merely describes a method of internal power estimation. Specifically, Khouja discloses here an internal power model defined to model energy which is consumed internal to a gate using input/output port characteristics. The model variables include input edge rates, output port toggle rates and output load capacitance (Khouja at col. 10, lines 60-66).

However, nowhere in this passage (nor anywhere else for that matter) does Khouja teach or suggest dividing a clock cycle into a plurality of time periods. Further, even assuming (arguendo) that Khouja suggests dividing a clock cycle into a plurality of time periods, Khouja certainly does not teach or suggest performing a static timing analysis for the plurality of cells to obtain current waveform data for each cell and each time period.

Applicant notes that an important purpose of the claimed invention is that it may perform a transient power distribution analysis. The claimed invention accomplishes this by dividing a CLOCK CYCLE (e.g., a single clock cycle) into multiple time periods (e.g., "buckets").

The prior art, on the other hand, is concerned with the average power condition. Importantly, a clock cycle is viewed as "atomic" by the other art. Thus, the prior art may be concerned with which circuits switch in a given clock cycle, but not when WITHIN a clock cycle.

This is a subtle but important difference. Unlike the conventional methods, the claimed invention may "break up" an individual clock cycle into a smaller unit of time (e.g., referred to in the present application as a "bucket").

For example, assume that a chip with 10 circuits is being examined. Further, assume that a designer wants to determine the power drawn by this chip over 2 consecutive clock cycles. The active (sometimes called dynamic) power of the chip is a function of which circuits switch and how often. Dynamic power is only consumed when a circuit switches.

Now assume that 5 circuits (out of the 10) switch on the first clock cycle and 6 on the second clock cycle. Part of the problem faced by the designer is determining those numbers (the 5 and 6 respectively). The prior art may be used to solve this problem.

The claimed invention, on the other hand, is also concerned with what is happening during an individual clock cycle. The prior art cannot be used to solve this problem.

For instance, in the above example, the claimed invention may determine when during the clock cycle each of the 5 circuits switched (e.g., looking at the first clock cycle) and/or when during the clock cycle the 6 circuits switched (e.g., on the second cycle). Thus, the claimed invention may be used to determine an instantaneous power supply collapse.

The prior art, on the other hand, is concerned only with an average power supply collapse. This is completely different from the claimed invention.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Khouja. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Standard Delay Format (SDF) Publication Reference

The Examiner alleges that the P1497 Draft Standard would have been combined with Khouja to form the claimed invention of claims 3, 20 and 32. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

The Standard Delay Format (SDF) publication discloses a textual file format for

representing the delay and timing information of electronic systems. SDF is a standard for the representation and interpretation of timing data for use at any stage of the electronic design process. SDF is intended to support timing models for modeling circuit delay, output pulse propagation, timing checks and interconnect delays (SDF publication at Abstract; pages 13-14)

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions.

Specifically, Khouja is directed to a method of computing the power dissipated in a digital circuit, whereas the SDF publication is merely directed to a method of representing and interpreting timing data. Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner merely states that it would have been obvious to combine the SDF publication with Khouja because the SDF publication "is the standard in the industry".

However, nowhere does Khouja even discuss the SDF publication. In fact, contrary to the Examiner's allegations, neither of these references teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, contrary to the Examiner's allegations, neither the SDF publication, nor Khouja, nor any combination thereof teaches or suggests "*performing a static timing analysis for said plurality of cells to obtain current waveform data for each cell and each time period*", as recited in claims 1 and 18, and similarly recited in claim 15.

As noted above, unlike conventional methods of analyzing power distribution, the claimed invention divides a clock cycle of the chip into a plurality of periods, divides the chip into a plurality of cells, and performs a static timing analysis for the plurality of cells to obtain

current waveform data for each cell and each time period (Application at page 11, lines 1-18). This allows the claimed invention to perform a transient power distribution analysis, unlike the conventional methods which are only concerned with an average power condition.

Clearly, the novel features of the claimed invention are not taught or suggested by the SDF publication. Indeed, the Examiner merely attempts to rely on the SDF publication as allegedly suggesting cell characterization data including charge data, timing data, voltage data, temperature data, load data, input slew rate data, direct current data and process corner data.

In fact, as noted above, the SDF publication merely discloses a method of representing and interpreting timing data. Indeed, the SDF publication is completely unrelated to the claimed invention which includes a method of analyzing power distribution.

Therefore, the SDF publication does not teach or suggest dividing a clock cycle of the integrated circuit chip into a plurality of time periods, let alone performing a static timing analysis for a plurality of cells to obtain current waveform data for each cell and each time period, as in the claimed invention. Therefore, the SDF publication clearly does not make up for the deficiencies of Khouja.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Fallah-Tehrani Reference

The Examiner alleges that Fallah-Tehrani would have been combined with Khouja to form the claimed invention of claims 5, 21 and 34. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Fallah-Tehrani discloses a method for static timing analysis of deep sub-micron devices in presence of crosstalk. The method attempts to provide an platform for fast and accurate static timing verification of large scale transistor and cell level netlists, with coupled interconnects and high switching speeds. The method also attempts to solve the coupled noise problem in static

timing verification.

Specifically, the method attempts to determine worst case aggressor switching time for a cross-coupled interconnect stage. After the worst case aggressor switching time is determined, the netlist is then resimulated using the worst case aggressor switching time to determine more accurate stage delay and slew of the interconnect state. The output waveform is recorded and utilized as the input of subsequent stages (Fallah-Tehrani at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions.

Specifically, Khouja is directed to a method of computing the power dissipated in a digital circuit, whereas Fallah-Tehrani is merely directed to static timing analysis. Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner merely states that it would have been obvious to combine Fallah-Tehrani with Khouja because "the effects of crosstalk in static timing analysis can be significant".

However, the Khouja method does not require static timing analysis (e.g., see Khouja at claim 1; col. 103, lines 1-32). In fact, contrary to the Examiner's allegations, neither of these references teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, contrary to the Examiner's allegations, neither Fallah-Tehrani, nor Khouja, nor any combination thereof teaches or suggests "*performing a static timing analysis for said plurality of cells to obtain current waveform data for each cell and each time period*", as recited in claims 1 and 18, and similarly recited in claim 15.

As noted above, unlike conventional methods of analyzing power distribution, the claimed invention divides a clock cycle of the chip into a plurality of periods, divides the chip

into a plurality of cells, and performs a static timing analysis for the plurality of cells to obtain current waveform data for each cell and each time period (Application at page 11, lines 1-18). This allows the claimed invention to perform a transient power distribution analysis, unlike the conventional methods which are only concerned with an average power condition.

Clearly, the novel features of the claimed invention are not taught or suggested by Fallah-Tehrani. Indeed, the Examiner merely attempts to rely on Fallah-Tehrani as allegedly suggesting extracting parasitic resistors, capacitors and inductors to generate extracted signal net information which is used to perform said static timing analysis.

In fact, as noted above, the Fallah-Tehrani merely discloses a method of static timing analysis, and is unrelated to the claimed invention which includes a method of analyzing power distribution.

Therefore, Fallah-Tehrani does not teach or suggest dividing a clock cycle of the integrated circuit chip into a plurality of time periods, let alone performing a static timing analysis for a plurality of cells to obtain current waveform data for each cell and each time period, as in the claimed invention. Therefore, Fallah-Tehrani clearly does not make up for the deficiencies of Khouja.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-40, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: 11/5/03

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CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner Brenda Bowers, Group Art Unit # 2825 at fax number (703) 872-9318 this 5th day of November, 2003.

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